In The Claims:

Please amend the claims as set forth below:

--66. (Currently amended) A mass-produced solid state device comprising:

a solid state material substrate having a top surface; and

a defect-free solid state material layer no more than ~~10 Angstroms~~ three atomic layers thick having at least one atomically smooth major surface, and positioned on the top surface of the substrate;

at least a central portion of the solid state material layer ~~being metallurgically bonded~~ has a non-flat major surface uniformly contacting intimately onto to at least a selected portion of the top surface of the solid ~~material~~ state material substrate ~~[to provide a thermochemically stable contacting surface interfacial region to avoid~~ production problem due to excessive leakage current.

67. (Currently amended) A solid state device as in claim 66 in which the solid state material layer has at least two of the following features: a) having an atomically ~~smoothed~~ smooth bottom surface; b) having a curved top surface; c) having an atomically ~~liquid-smoothed~~ smooth ~~gate~~ bottom gate layer; d) ~~made of purified material; e)~~ made of a single strengthened material; ~~f~~ e) accurate to one atomic layer in thickness; ~~g~~ f) is of an aged device material ~~aged by liquid diffusion; i~~ g) is atomically fine-grained ~~or subgrained; j)~~ h) have has oriented grains ~~or subgrains~~; k) i) ~~narrow grains or subgrains; and l~~ j) is stronger than ~~unbonded~~ uncontacted device material; and ~~l)~~ k) less than two atomic layers thick.

68. (Currently amended) The device as in claim 66 in which the solid state material layer has a central portion of zero bottom width ~~which is symmetrical with respect to a central vertical bisecting plane thereof.~~

69. (Currently amend d) Th device as in claim 66 in which the solid state mat rial layer has no flat ar a at its bottom, but has an accuracy of better than a single atom ~~several atoms~~ on a layer dimension selected from the group consisting of thickness, depth, curvature, shape, size, chemical composition profiling, and lateral location.

70. (Currently amended) The device as in claim 66 in which at least a portion of the solid state material layer ~~contains solid reinforcements~~ is surfaced strengthened, whereby the ~~bonded~~ uniformly intimately contacted solid state material layer is stronger than the ~~unbonded~~ uncontacted solid state material itself.

71. (Previously amended) The device as in claim 66 in which the solid state material layer is sufficiently thin and flexible so as to yield under stress preventing device failure.

72. (Currently amended) The device as in claim 66 in which the solid state material layer is ~~liquid-diffusion~~ of an aged or burned-in solid state material.

73. (Currently amended) The device as in claim 66 having a thickness of less than ~~a micron~~ three atomic layers thereby forming a ~~flexible~~ thin-film integrated circuit device.

74. (Currently amended) The device as in claim 66 wherein the solid state material layer has a curved major surface with a radius of curvature of less than ~~1 micron~~ 0.5 microns..

75.(Currently amended) The device as in claim 66 in which material of the solid state material layer is ~~purified by a melting and solidification process;~~

~~the purity of material of the solid state material layer being improved by~~ at least one order of magnitude purer than ~~relative to~~ the solid state material prior to said

81. (Previously added) The device as in claim 66 in which the substrate material is select d from the group consisting of Si, Ge, Si-Ge, InP, InSb, GaAs, SiC, InAs, superconductor, diamond, semiconductor material, intrinsic semiconductor material, substantially electrically insulating material, and substantially electrically conducting material, and mixture thereof.

82. (Currently amended) The device as in claim 66 selected from the group consisting of metal-oxide-semiconductor (MOS) device, conductor-insulator-semiconductor (CIS) device, thin-film integrated circuit, ~~and~~ flexible integrated circuit, electro optical device, electrooptomagnetic devices and mixtures thereof.

83.(Currently amended) The device as in claim 78 in which:

the first and second solid state material pockets are respectively source and drain semiconductor pockets in a ~~[CMOS]~~ solid-state device and separated by a gap from each other; the solid state material layer is ~~a~~ an insulating gate layer filling and bridging the gap between the two pockets; and

the gate layer material has an atomically smooth surface ~~at least~~ on at least one of the top and ~~major~~ bottom major surfaces thereof.

84. (Currently amended) The device as in claim 83 in which each of a major portion of the substrate, solid state material pockets, and solid state material layer consists essentially of a single ~~doped and less doped intrinsic~~ semiconductor material doped to no more than 10 ppm of impurities whereby the device is made resistant to dynamic forces due to impacts, vibrations, and large and rapid accelerations and decelerations.

85. (Currently amended) The device as in claim 66 including a PN junction region having a curved adjoining surface without any flat bottom thereon, and contacting the substrate to thereby reduce but not eliminate at least one of ~~inevitable~~ thermal mismatch stress and ~~in situ~~ volume change strain ~~generated during device~~

~~processing~~;

the remaining residual strain and stress on the curved adjoining surface of the PN junction region improving a selected device performance.

86. (Currently amended) The device as in claim 79 in which:

the at least one PN junction region has a curved adjoining surface without a flat ~~[portioon]~~ portion thereon and;

the at least one of the first and the second solid state material pockets meets the curved adjoining portion of the at least one PN junction region.

87. (Cancelled).

88. (Currently amended) The device as in claim 66 in which the solid state material layer is an electrically insulating, ~~wavy and~~ curved field layer containing ~~an ion-implanted~~ a substance selected from the group consisting of oxygen and nitrogen.

89. (Currently amended) The device as in claim 78 in which:

the first and second solid state material pockets are respectively source and drain semiconductor pockets in a ~~CMOS~~ solid state device; and

the solid state material layer is a single-material gate layer; and

including a conductive gate electrode of an electrically conducting material positioned on the gate layer to control flow of electronic carriers from the source to the drain.

90. (Currently amended) The device as in claim 89 in which:

the gate layer material is atomically ~~smoothed~~ smooth on at least one of top and bottom major surfaces thereof to achieve ~~maximum smoothness~~ exceptionally smooth and defect-free surface; and

material of the gate layer being ~~most purified~~ purest at a bottom surface facing

the substrate.

91. (Previously added) The solid state device as in claim 66 in which:

the solid state material layer is a field layer separating and electrically isolating device components from each other on the substrate;

the field layer on a horizontal cross-section thereof has a plurality of curved sections; and

each curved section has an arc length defined by: l = r x A where l is the arc length, r is the radius of curvature of the arc, and A is the subtended arc angle;

each arc section being capable of flexing whereby the arc length is changed by delta l = r x delta A + A x delta r; and

the changes in delta l, delta r, and delta A all being in directions to reduce thermal mismatch strain and automatically stopping when the residual thermal mismatch strain is reduced by the changing arc length to a point such that the multiply curved field layer can tolerate without failure the residual thermal mismatch strain.

92. (Previously amended) The solid state device as in claim 66 in which the solid state material layer is curved to minimize thermal mismatch stresses.

93. (Currently amended) A mass-produced solid state device comprising:

a solid state material substrate;

at least one first solid state material pocket positioned on a first selected top surface of the substrate; and

a solid state material layer less than three atomic layers thick and having at least one atomically smooth but curved major surface which intimately contacts ~~and metallurgically bonds~~ uniformly the first selected surface of the substrate ~~to~~ onto a first specified portion of the at least one first solid state material pocket.

94. (Currently amended) A solid state device as in claim 93 in which the at least one atomically smooth but curved major surface intimately contacts uniformly, atom to

atom, the first selected surface of th substrate onto said first specified portion of the at l ast one first solid state material pocket; and furth r comprising:

a second solid state material pocket positioned on a second selected surface of the substrate, and laterally adjacent to, but separated by a gap from, the at least one first solid state material pocket; and in which:

the solid state material layer fills the gap between the two material pockets while intimately contacts ~~and metallurgically bonds~~ uniformly with a second specified portion of the second solid state material pocket.

95. (Currently amended) A mass-produced solid state device comprising:

a solid state material substrate;

a left and a right adjacent solid state material pockets laterally separated by a gap and positioned on a common top surface of the substrate;

a curved solid state material layer which: a) is less than 40 angstroms thick; ~~and~~ b) is positioned on the common top surface of the substrate to bridge the gap between the two solid state material pockets ~~pocket~~; c) has a rounded bottom; and d) is a single-material solid state material layer selected from the group consisting of gate layer and field layer.

96. (New) the solid state device as in claim 93 in which the solid state material layer is curved and has a rounded bottom of ~~zero~~ width to minimize thermal mismatch stresses.

97. (New) The solid sate device as claimed in claim 95 in which the solid sate state material layer is concavely curved when viewed from a top view.

98. (New) The device as in claimed in claim 93 in which the solid state material layer is a single-material gate layer containing a substance selected from the group consisting of oxygen and nitrogen.

99. (New) Th device as in claim d in claim 79 in which ~~said~~ the PN junction region has a ~~[very shallow]~~ d pth of less than 70 nonometers.